

Attorney Docket No.: 0140105

REMARKS

By the present amendment and response, claims 1-9 and 17-20 have been amended to overcome the Examiner's objections. Claims 1-20 are pending in the present application. Reconsideration and allowance of pending claims 1-20 in view of the above amendments and the following remarks are requested.

The Examiner has rejected claims 1-20 under 35 USC §102(b) as being anticipated by U.S. Patent No. 6,404,289 to Su et al. (hereinafter "Su"). For the reasons discussed below, Applicants respectfully submit that the present invention, as defined by the amended independent claims 1, 9 and 17, is patentably distinguishable over Su.

The present invention, as defined by amended independent claims 1, 9 and 17, includes a coarse tuning circuit coupled to a voltage controlled oscillator, where the coarse tuning circuit is further coupled to a phase locked loop which is in turn connected to a loop filter, where the loop filter generates a fine tuning voltage for use by the voltage controlled oscillator. The coarse tuning circuit (for example, coarse tuning circuit 302 in Figure 3 of the present application) includes a lock detect monitoring circuit which detects the state of the phase locked loop and provides this state information to an autotuner circuit inside the coarse tuning circuit. A VTUNE monitoring circuit monitors an output of the loop filter and provides fine tuning information to the autotuner circuit. The autotuner circuit can then provide coarse tuning information to the voltage controlled oscillator.

Attorney Docket No.: 0140105

The disclosed and claimed invention comprising the novel use of a phase locked loop and loop filter to provide state and fine tuning information to a coarse tuning circuit is not taught, disclosed, or suggested by Su. Further, a coarse tuning circuit including a lock detect monitor, VTUNE monitoring circuit, and an autotuner circuit is not taught, disclosed, or suggested by Su.

Su merely discloses lock detect circuit 300 including OR gate 310, AND gate 320, delay circuit 330, flip flop 340, reset OR gate 350, latch circuit 360, counter 370, and lock output circuit 380. See, e.g., column 4, lines 22-27 and Figure 3 of Su. As such, many of the elements and interconnections disclosed and claimed by the present invention are not disclosed or suggested by Su. Although Su appears to disclose establishing a lock condition with a selected "characteristic curve," such characteristic curve is utilized to reduce "phase noise." See, e.g., column 8, lines 11-17. However, the invention teaches and claims use of tuning curves to achieve fine tuning in a novel manner to overcome various shortcomings in the art. For example, in accordance with the invention, the previously existing need to disconnect the phase locked loop and/or the loop filter from the voltage controlled oscillator during coarse tuning is avoided. See, for example, page 18, lines 1-2 of the present application.

More fundamentally, the present invention is directed to a block diagram and a circuit arrangement that are not taught, disclosed or suggested by Su, regardless of the differences or any similarities of the general results achieved by the present invention or Su. In other words, the block diagram and circuit claimed by the present invention are

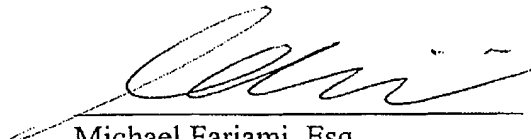
Attorney Docket No.: 0140105

not taught, disclosed, or suggested in Figure 3 of Su, or any other Figure or description in Su. As such, the present invention, as claimed by the present amended claims, is patentably distinguishable over Su. Thus, an early notice of allowance directed to pending claims 1-20 is respectfully requested.

Attorney Docket No.: 0140105

Respectfully Submitted,
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Date: 1/20/05


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